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L31: Entry 1 of 2 File: USPT Jul 29, 2003

DOCUMENT-IDENTIFIER: US 6601177 B1
TITLE: Semiconductor integrated circuit

Brief Summary Text (2):
The present invention relates to a semiconductor integrated circuit having many internal circuits. More particularly, this invention relates to a semiconductor integrated circuit which can realize lower power consumption by driving the internal circuits using a plurality of power supply voltages.

Brief Summary Text (4):
In recent years, lower power consumption of a semiconductor integrated circuit (henceforth, LSI) has been demanded in association with enhanced performance of mobile equipment. As a conventional LSI that allows low power consumption to be realized, there has been known one that uses a plurality of power supply voltages for circuit groups (internal circuits) of the LSI. FIG. 7 schematically shows a configuration of such a conventional LSI. This LSI 91 comprises a plurality of circuit groups 92 (1) to 92 (n) (where n is an integer), a plurality of power supply external terminals 93 (1) to 93 (n) that receive a plurality of power supply voltages VDD (1) to VDD (n) used for the circuit groups 92 (1) to 92 (n), and an external terminal 94 for a ground.

Detailed Description Text (5):
The DACs 6 (1) to 6 (n) operate by a power supply voltage VDD input via the external terminal 4 used for turning the power on, generate analog signals based on the digital signals from the registers 7 (1) to 7 (n), and provide the generated analog signals as power supply voltages VDD (1) to VDD (n) to the circuit groups 2 (1) to 2 (n). Each of the registers 7 (1) to 7 (n) is a nonvolatile memory such as flash memory, stores a digital value according to the setting from the CPU 8, and outputs a digital signal based on the stored digital value to each of the DACs 6 (1) to 6 (n).

Current US Original Classification (1):
713/300

L32: Entry 1 of 1 File: USPT Oct 31, 2000

DOCUMENT-IDENTIFIER: US 6141761 A
TITLE: Low power consuming operating device for digital signal processing using a probability distribution of input digital signals and predetermined output signals

Detailed Description Text (2):
FIG. 1 is a block diagram of an operating device according to the present invention. The operating device has an external input portion 10, a specified signal sensing portion 12, an internal input portion 14, an operating portion 16, and an external output portion 18. In FIG. 1, the external input portion 10 receives digital data via an input port IN, temporarily stores the digital data, outputs the stored digital signal to the specified signal sensing portion 12 and the internal input portion 14. The specified signal sensing portion 12 determines whether the digital data received from the external input portion 10 is a specified input, and outputs the result as a control signal for the internal input portion 14 and the external output portion 18. The internal input portion 14 receives the digital data from the external input portion 10 in response to the determination result, and outputs the digital data to the operating portion 16 or maintains a previous output value. That is, the value of the data output from the internal input portion 14 to the operating portion 16 is varied in response to the determination result.

Detailed Description Text (7):
An investigation of IDCT inputs in MPEG shows that 30% or more of the inputs are only `0s` and in some cases 50% are `0s`. Here, use of the operating device of the present invention can reduce power consumption remarkably. That is, since the values of signal lines in the operating portion 16 experience no variation, if the operating portion 16 is comprised of CMOS, power consumption can be markedly reduced. This is because most of the power consumption in a CMOS circuit is dynamic power consumption incurred when a signal value varies. In addition, the specified input is sensed and its corresponding output is immediately generated, thereby increasing the average operation speed of the system.

Detailed Description Text (24):
Meanwhile, a validity signal is output via the output terminal OUT2 to indicate that the signal output via the output terminal OUT1 is valid or not. The operating device of FIG. 6 uses a gated clock signal and has the specified signal sensing portion 102 for sensing the specified input `0`, as compared with the operating device of FIG. 5.

Detailed Description Text (25):
Assuming that the operating devices of FIGS. 5 and 6 use the same internal operating portion in terms of structure and operation, the latter operating device is smaller than the former in circuit size since the latter adopts a gated clock method, thus needing no multiplexers in an input portion. Both multipliers will be compared under the following four conditions:

Detailed Description Text (27):
Condition 2. When neither input is `0` and an operation is not always necessary,

the operating device of the present invention shows a 15% decrease in power consumption, since it uses a gated clock method. This assumes that the operating device operates 80% of the time. However in a real application, the operating device does not operate for even 10% of the time, as compared with the system. Therefore, a greater decrease of power consumption can be expected in a real situation;

Detailed Description Text (28):
Condition 3. When one of the two inputs is `0`, power consumption of the multiplier of the present invention was decreased by about 80%, which implies that 80% of consumed power can be saved in this condition compared to the above conditions; and

Detailed Description Text (32):
The present applicant compared the operating devices of FIGS. 5 and 6 under the following conditions as shown in table 1.

Current US Original Classification (1):
713/300

Current US Cross Reference Classification (2):
713/320

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L11: Entry 1 of 1 File: USPT Dec 25, 2001

DOCUMENT-IDENTIFIER: US 6333954 B1
TITLE: High-speed ACS for Viterbi decoder implementations

Brief Summary Text (7):
FIG. 1A illustrates a typical convolutional encoder. The convolutional encoder 100 comprises an 8-bit tapped shift register 110 and a pair of exclusive OR-type summers 120 that transform a sequence of input data bits U(D) 105 into a sequence of output code symbols C.sub.0 (D), C.sub.1 (D) 125. In particular, FIG. 1A demonstrates the example of a rate.sub.13 code which generates two output coding symbols C.sub.0 (D), C.sub.1 (D) 125 for each input data bit U(D) 105. It is to be noted that the specific code rate and configuration of the convolutional encoder 100 shown is merely illustrative and in no way limits the operation or scope of the various embodiments of the invention. As such, different code rates, such as 1/3or _, for example, could be used in conjunction with the embodiments of the invention.

Brief Summary Text (21):
For each of the two target states, the ACS 150 compares the sum of the source state metric-branch metric pairs leading to that target state. The most likely transition into each target state, represented by the smallest metric sum, is then "selected" by ACS 150 and assigned to that target state as the target state metric tm.sub.0x, tm.sub.1x.

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L14: Entry 1 of 1 File: USPT Dec 31, 2002

DOCUMENT-IDENTIFIER: US 6501860 B1
TITLE: Digital signal coding and decoding based on subbands

Brief Summary Text (2):
The purpose of coding is to compress the signal, which enables the digital signal to be transmitted, or respectively stored, thus reducing the transmission time or transmission rate, or respectively reducing the memory space used.

Detailed Description Text (44):
The path is optimal in the sense of a cost which is minimised over the entire trellis, and therefore over the entire series to be coded. The cost of a transition is the quadratic error measured between the symbol to be coded and the code vector selected in the dictionary identified by the state in which the transition ends up. The cost of a state of the trellis is the sum of the costs of the transition leading to this state. The Viterby algorithm calculates the minimum cost of each state in order to determine the optimum path represented by the series of transitions i(k).

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L9: Entry 5 of 7 File: USPT Feb 28, 1995

DOCUMENT-IDENTIFIER: US 5394106 A
TITLE: Apparatus and method for synthesis of signals with programmable periods

CLAIMS:

2. A digital synthesizer for synthesizing an output signal having one or more user programmable periods comprising:

a system clock for providing a clock signal;

an N bit magnitude comparator circuit having first and second compare inputs, each for receiving an N bit digital word, where N is any integer, said magnitude comparator circuit for comparing the magnitudes of said N bit digital words appearing at said first and second compare inputs, and having an output at which a strobe signal transitions to an active state when the magnitudes of said N bit digital words appearing at said first and second compare inputs are equal, said strobe signal comprising said synthesized output signal from said digital synthesizer;

an accumulator circuit having a data input and a data output, the present value of said accumulator appearing at said data output, said accumulator circuit also having a strobe input coupled to receive said strobe signal from said magnitude comparator circuit, and having a clock input for receiving clock signals from said system clock, both said data input and said data output of said accumulator being M+N bits wide, wherein M and N are integers of any selected value, and N represents the N most significant bits presented at either said data input or said data output of said accumulator, and M represents the M least significant bits, said data input of said accumulator circuit serving to receive a digital input word, U, said accumulator for adding said digital input word, U, to the present value of said accumulator upon receipt of the next clock signal after said strobe signal from said magnitude comparator circuit transitions to said active state, with the resulting sum being presented at said data output of said accumulator, only said N most significant bits appearing at said data output of said accumulator being coupled to said first compare input of said magnitude comparator circuit, and wherein said M least significant bits at said data output are unconnected but effect the value of said N most significant bits through internal carry operations occurring within said accumulator;

an N bit synchronous counter having a clock input coupled to receive clock signals from said system clock, and having an N bit wide data output coupled to said second compare input of said magnitude comparator circuit, said synchronous counter for incrementing a count upon receipt of each clock signal and presenting said count as an N bit digital word at said second compare input;

an input coupled to said data input of said accumulator for receiving said digital input word, U, comprised of N most significant bits and M least significant bits.

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L9: Entry 7 of 7 File: DWPI Nov 22, 1990

DERWENT-ACC-NO: 1990-350423
DERWENT-WEEK: 199649

TITLE: Circuit which implements viterbi algorithm - has states of defined time intervals, processed in serial form indicating symbol of one or more bits regardless of states

Equivalent Abstract Text (1):
Circuitry implementing the Viterbi algorithm in a trellis in which each state may be entered along two alternative paths, and the states of the bits of a defined time interval are processed with the circuitry in serial form for indicating the symbol of a bit and/or several bits, the circuitry comprising: (a) addition circuits (ADD) operable, for each bit (BITk), to calculate addition values of each potential next state from the sum of the transition values (TRANSk) and the cumulative values (CUM(i)) of the states at each moment; (b) comparison means by which the two addition values of each state are compared; (c) a trace back path table (TB) storing the result of comparison; and (d) a selection circuit selecting a new cumulative value (NEW) and storing it in the table of cumulative values (CT) characterised in that the comparison means comprises a subtraction circuit (SUB) producing a comparison result in the form of a number of bits.

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L9: Entry 2 of 7 File: USPT Jul 8, 2003

DOCUMENT-IDENTIFIER: US 6590939 B1
TITLE: Reception method and a receiver

Brief Summary Text (2):
The invention relates to a reception method in which received symbols are functions of bits, which are detected at successive trellis levels A and B by adding to a sum of a transition metric of each path that has led to each state of the level A a transition metric of a path branch relating to a bit 1 and a bit 0 and leading to the next level B and; by comparing at the level B that follows the level A the sums of the transition metrics of path branches entering each state; and by selecting, on the basis of the sums of the transition metrics, in each state of the level B the best of the two paths as a survivor path.

Brief Summary Text (3):
The invention also relates to a reception method in which received symbols are functions of bits, which are detected at successive trellis levels A and B by adding to a sum of a transition metric of a path that has led to each state of the level A a transition metric relating to a bit 1 and a bit 0 and leading to the next level; by comparing the sums of the transition metrics of path branches entering each state at the level B that follows the level A; and by selecting, on the basis of the sums of the transition metrics, in each state of the level B the best of two paths as a survivor path.

Brief Summary Text (4):
The invention further relates to a receiver, which comprises means for forming a transition metric of a trellis, the means being used for determining bits relating to received symbols; and selecting means for adding to the sum of the transition metric of each path that has led to each state of the level A, of the two successive levels A and B, a transition metric of two path branches leading to the next level B; for comparing at the level B that follows the level A the sums of the transition metrics of the path branches entering each state; and for selecting, on the basis of the sums of the transition metrics, in each state of the level B the best of the two paths as a survivor path.

Brief Summary Text (5):
The invention further relates to a receiver comprising means for forming the transition metric of the trellis, the means being used for determining the bits relating to the received symbols; and selecting means for adding to the sum of the transition metric of each path that has led to each state of the level A, of the levels A and B, the transition metric of the two path branches leading to the next level; for comparing the sums of the transition metrics of the path branches entering each state at the level B that follows the level A; and for selecting, on the basis of the sums of the transition metrics, in each state of the level B the best of the two paths as a survivor path.

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L9: Entry 4 of 7 File: USPT Feb 17, 1998

DOCUMENT-IDENTIFIER: US 5719843 A
TITLE: Method of maximum likelihood decoding and digital information playback apparatus

CLAIMS:

2. The maximum likelihood decoder according to claim 1 wherein said maximum likelihood decoding means comprises a branch metric calculator, an addition comparison selector, a survival path detector, and a smoother, and wherein said branch metric calculator obtains the cumulative sums of the absolute values of differences between the quantized data values of said playback signal and expected values of partial response equalization output from said smoother, and said addition comparison selector selects most likely state transitions using said cumulative sums.

4. The maximum likelihood decoder according to claim 1 wherein said maximum likelihood decoding means comprises a branch metric calculator, an addition comparison selector, a survival path detector, and a smoother, and wherein said branch metric calculator obtains the cumulative sums of the squares of differences between the quantized data values of said playback signal and expected values of partial response equalization output from said smoother, and said addition comparison selector selects most likely state transitions using said cumulative sums.

6. The maximum likelihood decoder according to claim 1 wherein said maximum likelihood decoding means comprises a branch metric calculator, an addition comparison selector, a survival path detector, and a smoother, and wherein said branch metric calculator switches expected equalized values between initially set values and output values of said smoother when obtaining the cumulative sums of distances between the quantized data values of said playback signal and expected values of partial response equalization output from said smoother, and said addition comparison selector selects most likely state transitions using said cumulative sums.

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L9: Entry 1 of 7 File: USPT Apr 13, 2004

DOCUMENT-IDENTIFIER: US 6721254 B1
TITLE: Drive device

Detailed Description Text (83):
In order to select a most likely state transition, it is required to calculate the sums of likelihood values of all transitions in paths to a state at a point in time k through a plurality of points in time, and then compare the calculated sums of likelihood values to select a series of most likelihood decoded data. The sum of likelihood values is referred to as a path metric.

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